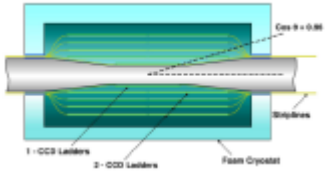
A CCD-based vertex detector



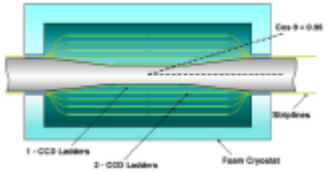
Report from the LCFI collaboration

Konstantin Stefanov

RAL

- Introduction: Conceptual design of the vertex detector for the future LC
- Detector R&D program at LCFI
  - Development of Column-Parallel CCDs and readout electronics
  - Experimental studies on a commercial high speed CCD
  - Thin ladder program for mechanical support of the sensors
- Summary

Detector parameters

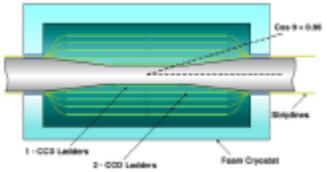


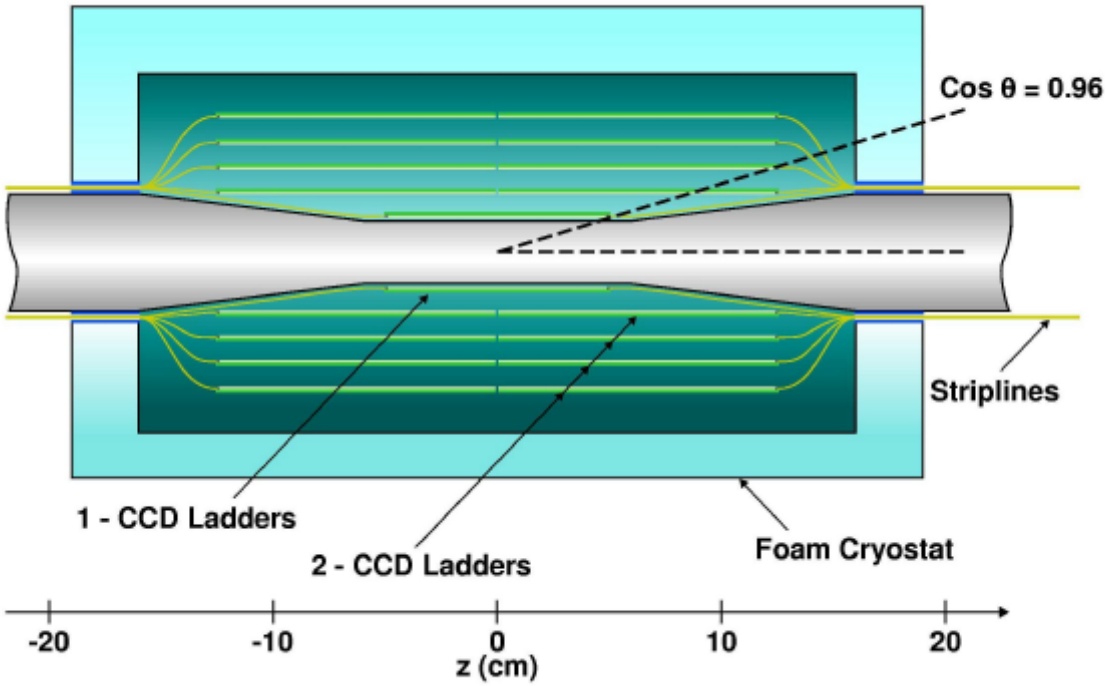
Several times better than the SLD VXD3 detector…

- Impact parameter resolution: $s = 4.2\,\text{Å} \dfrac{4.0}{p \sin^{3/2} q}$, [μm]
- Thin detector (< 0.1% X_0) for low error from multiple scattering
- Close to the interaction point for reduced extrapolation error
- Readout time: » 8 ms for NLC/JLC (read between trains)

  50 μs for TESLA (read the inner layer »20 times during the train)
- Pixel size » 20 μm ´ 20 μm;
- Large polar angle coverage;
- Stand-alone tracking: 4 or 5 layers of sensors;
- Radiation hard.

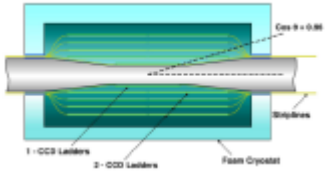
Conceptual design





- 5 layers at radii 15, 26 37, 48 and 60 mm;
- Gas cooled;
- Low mass, high precision mechanics;
- Encased in a low mass foam cryostat;
- Minimum number of external connections (power + few optical fibres).

CCD development



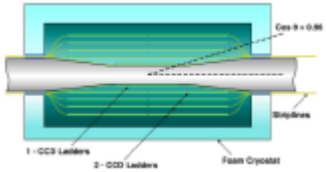
Large area, high speed CCDs

- Inner layer CCDs: 100´13 mm², 2500(V)´650(H) pixels per CCD end;
- Outer layers: 2 CCDs with size 125´22 mm² , 6250(V)´1100(H) pixels per CCD end;
- 120 CCDs, 799´10⁶ pixels in total;
- For NLC/JLC : readout time » 8 ms in principle sufficient, but not easy to achieve with standard CCDs;
- For TESLA :
  - 50 μs readout time for inner layer CCDs : 50 Mpix/s from each CCD column
  - Outer layers: 250 μs readout, 25 MHz from each column

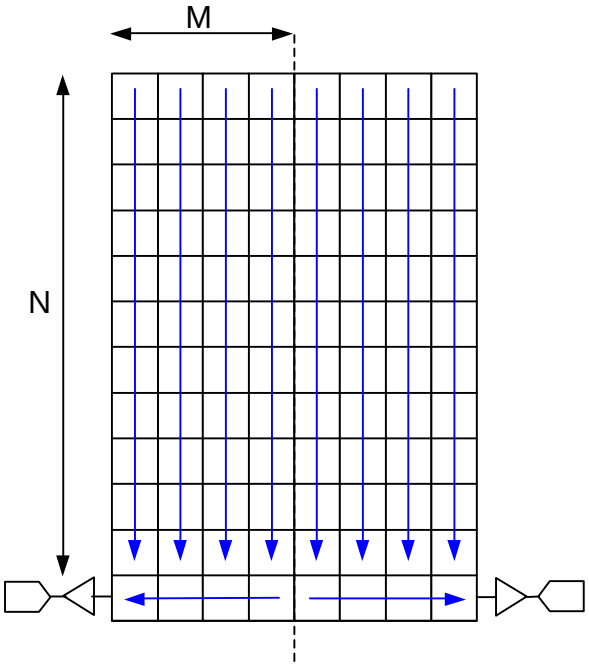
High speed requires different concept for fast readout – Column Parallel CCD (CPCCD)

Natural and elegant development of CCD technology

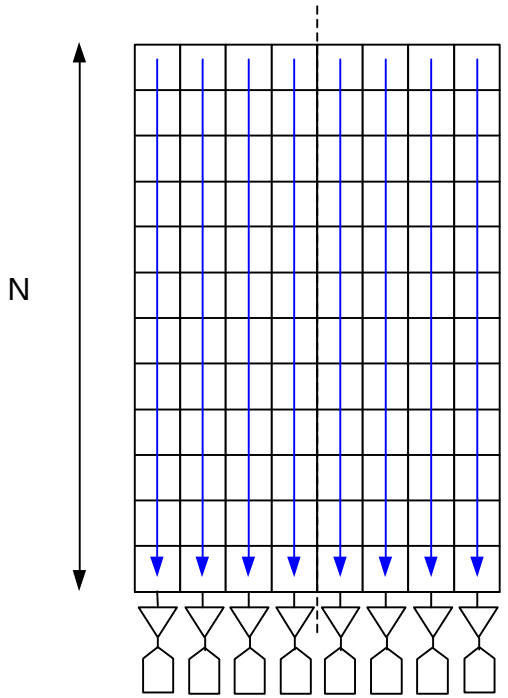
Column parallel CCD



- **Serial register is omitted**
- **Maximum possible speed from a CCD (tens of Gpix/s)**
- **Image section (high capacitance) is clocked at high frequency**
- **Each column has its own amplifier and ADC – requires readout chip**

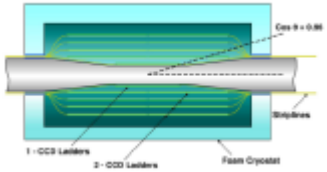


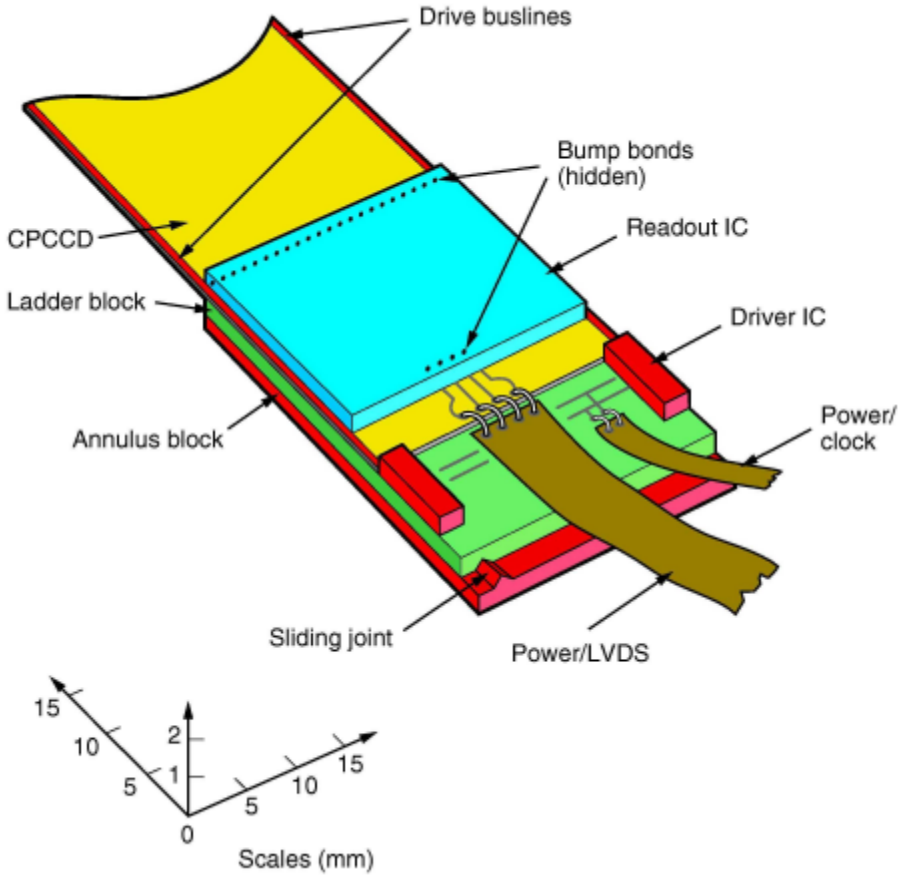
“Classic CCD”
Readout time ≈ $N \times M / F_{out}$



Column Parallel CCD
Readout time = N / F_{out}

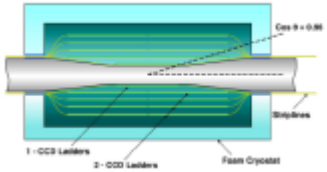
CCD ladder end



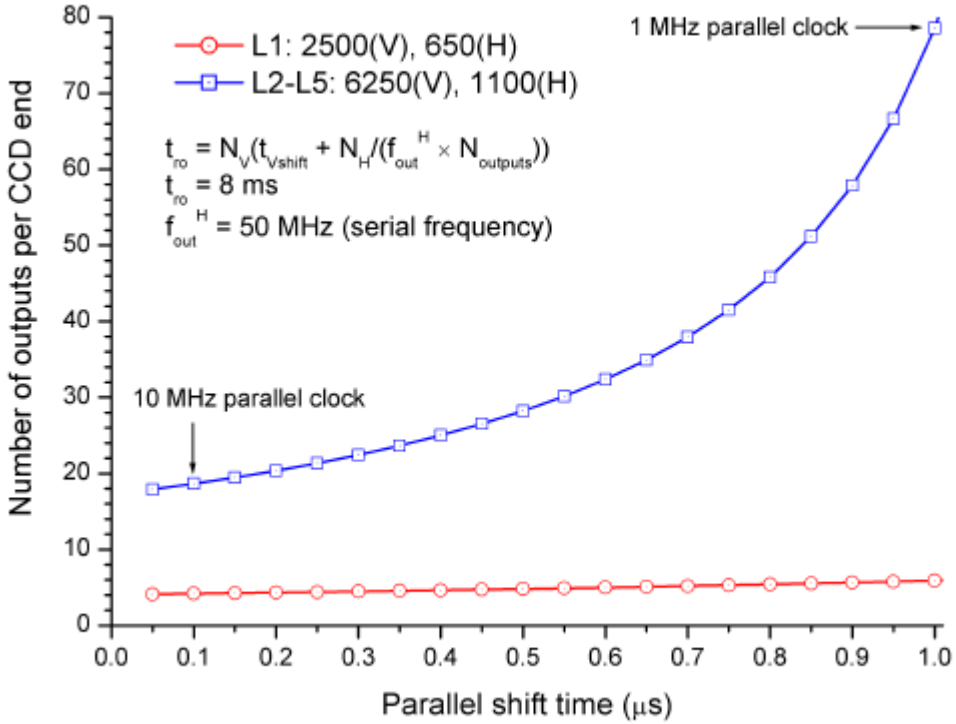


- **Electronics only at the ends of the ladders;**
- **Bump-bonded assembly between thinned CPCCD and readout chip;**
- **Readout chip does all the data processing:**
  - ♦ Amplifier and ADC with Correlated Double Sampling for each CCD column
  - ♦ Gain equalisation between columns
  - ♦ Hit cluster finding
  - ♦ Data sparsification
  - ♦ Memory and I/O interface
- **CPCCD is driven with high frequency, low voltage clocks;**
- **Low inductance layout for clock delivery.**

CCDs for NLC/JLC



CCDs for NLC/JLC machines



Multiple outputs considered for 8 ms readout time:

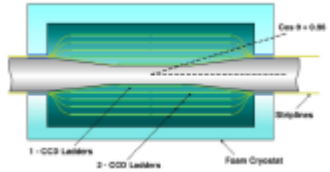
- **L1: » 6 outputs/CCD end**
- **L2-L5: High parallel clock frequency required**
  - **Standard technology: » 80 outputs @ 50 MHz, 1 μs parallel shift time;**
  - **» 20 outputs @ 50 MHz at 0.1 μs parallel shift time;**
  - **Readout chip very desirable**

CCDs for L2-L5 may need high speed features as in the CPCCDs for TESLA:

- **Gate metallization, low clock amplitudes;**
- **Low inductance bus lines, clock driver;**

The same readout time achievable with CPCCD at 1.28 μs parallel shift time (780 kHz).

Column Parallel CCD



Important aspects of the CPCCDs for TESLA:

Quality of 50 MHz clocks over the entire device (area = 13 cm^2):

- **All clock paths have to be studied and optimised**

Power dissipation:

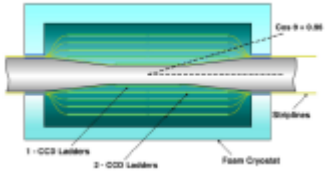
- **Low average power (» 10 W) for the whole detector, but large peak power (duty cycle = 0.5%);**
- **Low clock amplitudes**
- **Large capacitive load (normally » 2-3 nF/cm^2)**

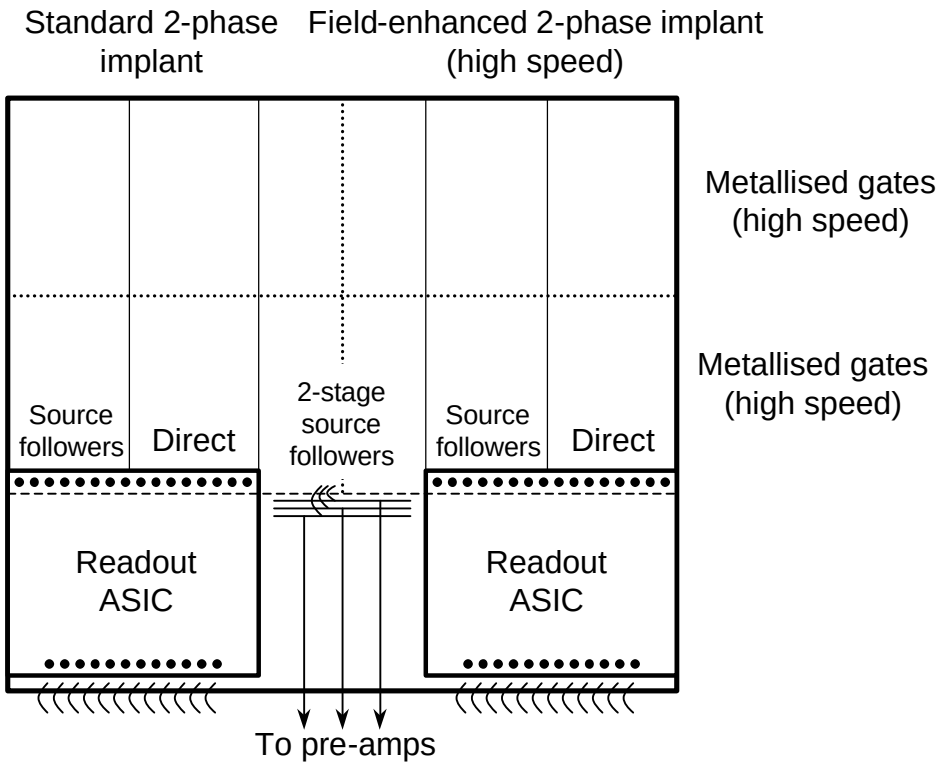
Feedthrough effects:

- **2-phase drive with sine clocks – natural choice because of symmetry and low harmonics**
- **Ground currents and capacitive feedthrough largely cancel**

Most of these issues are being studied by device simulations

Hybrid assembly CPCCD-CMOS

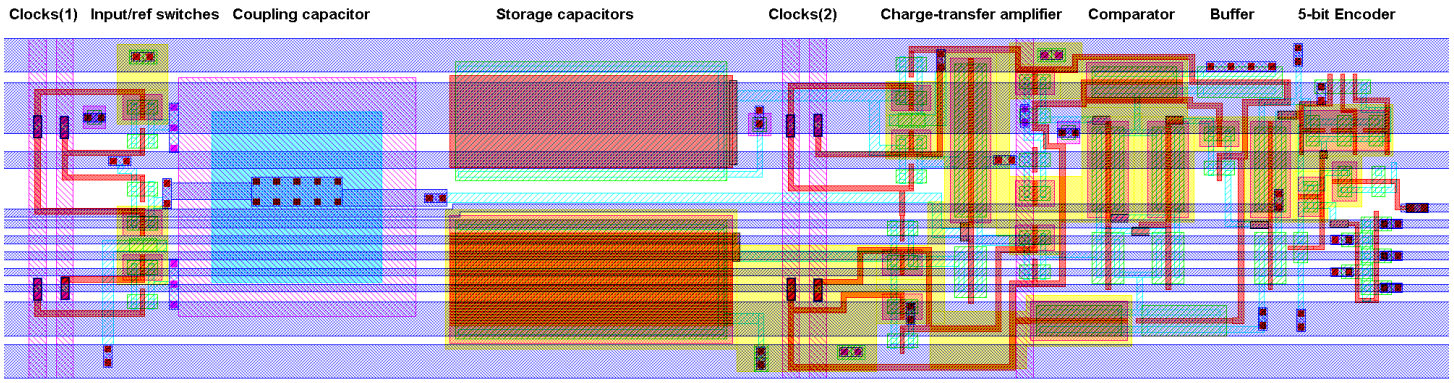




Features in our first CPCCD:

- **2 different charge transfer regions;**
- **3 types of output circuitry;**
- **Independent CPCCD and readout chip testing possible:**
  - **Without readout chip - use external wire bonded electronics;**
  - **Without bump bonding - use wire bonds to readout chip;**
  - **CPCCD bump bonded to readout chip;**
- **Different readout concepts can be tested.**

Readout chip design



A comparator using Charge Transfer Amplifier, repeated 31 times per ADC

- Readout chip designed by the Microelectronics Group at RAL;
- 0.25 µm CMOS process; scalable and designed to work at 50 MHz.

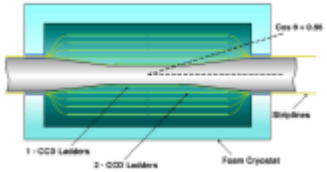
CPR-0 :

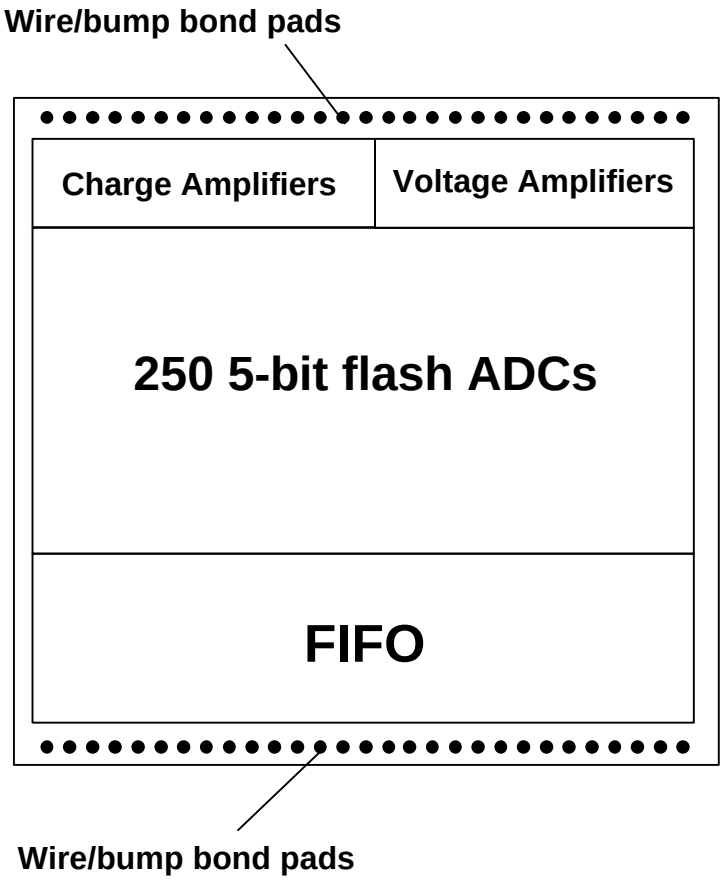
- Small chip (2 mm ´ 6 mm) for tests of the flash ADC and voltage amplifiers;
- Successfully tested at 50 MHz, results applied to the next design;

CPR-1 :

- Bump-bondable to the CPCCD;
- Contains amplifiers, 250 5-bit ADCs and FIFO memory in 20 µm pitch;
- Design almost completed.

Readout chip design





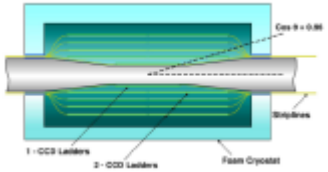
In CPR-1:

- **Voltage amplifiers – for source follower outputs from the CPCCD**
- **Charge amplifiers – for the direct connections to the CPCCD output nodes**
- **Amplifier gain in both cases: 100 mV for 2000 e- signal**
- **Noise below 100 e- RMS (simulated)**
- **Correlated Double Sampling built-in in the ADC**

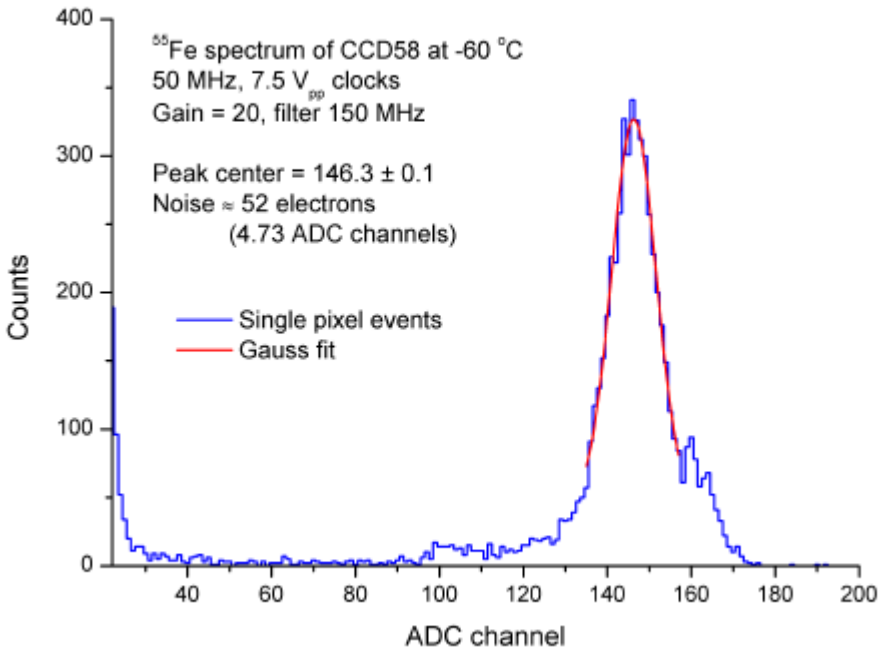
Direct connection and charge amplifier have many advantages:

- **Eliminate source followers in the CCD;**
- **Reduce total power to » 1 mW/channel, no active components in the CCD;**
- **Programmable decay time constant (baseline restoration).**

Tests of high-speed CCDs



^{55}Fe X-ray spectrum at 50 Mpix/s



Test bench for high-speed operation with MIP-like signals

E2V CCD58 :

- 3-phase, frame transfer CCD
- 2.1 million pixels in 2 sections
- 12 µm square pixels

◆ MIP-like signal (» 1620 electrons);

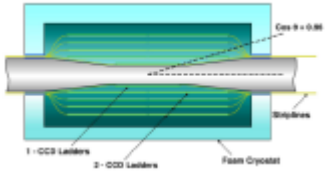
◆ Low noise » 50 electrons at 50 MHz;

◆ CCD58 is designed to work with large signals at 10 V_{pp} clocks;

  ◆ No performance deterioration down to 5 V_{pp} clocks;

  ◆ Still good even at 3 V_{pp} clocks.

Tests of high-speed CCDs



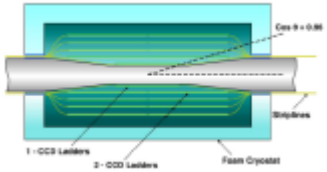
Radiation damage effects important for overall detector design

- **Influence operating temperature, readout frequency, CCD design**

Backgrounds:

- **» 50 krad/year (e^+e^- pairs)**
- **» 10^9 neutrons/cm^2/y (large uncertainty)**
- **Bulk radiation damage effects on CCD58 being studied:**
  - **Charge Transfer Inefficiency (CTI) – important CCD parameter**
  - **How radiation-induced CTI behaves with temperature and serial frequency in the range 1 – 50 MHz;**
- **CTI should improve a lot at speeds > 5-10 Mpix/s – to be verified;**

Thin ladder R&D



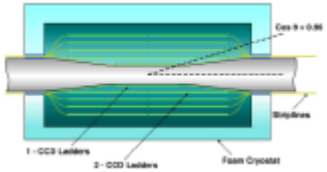
A program to design CCD support structures with the following properties:

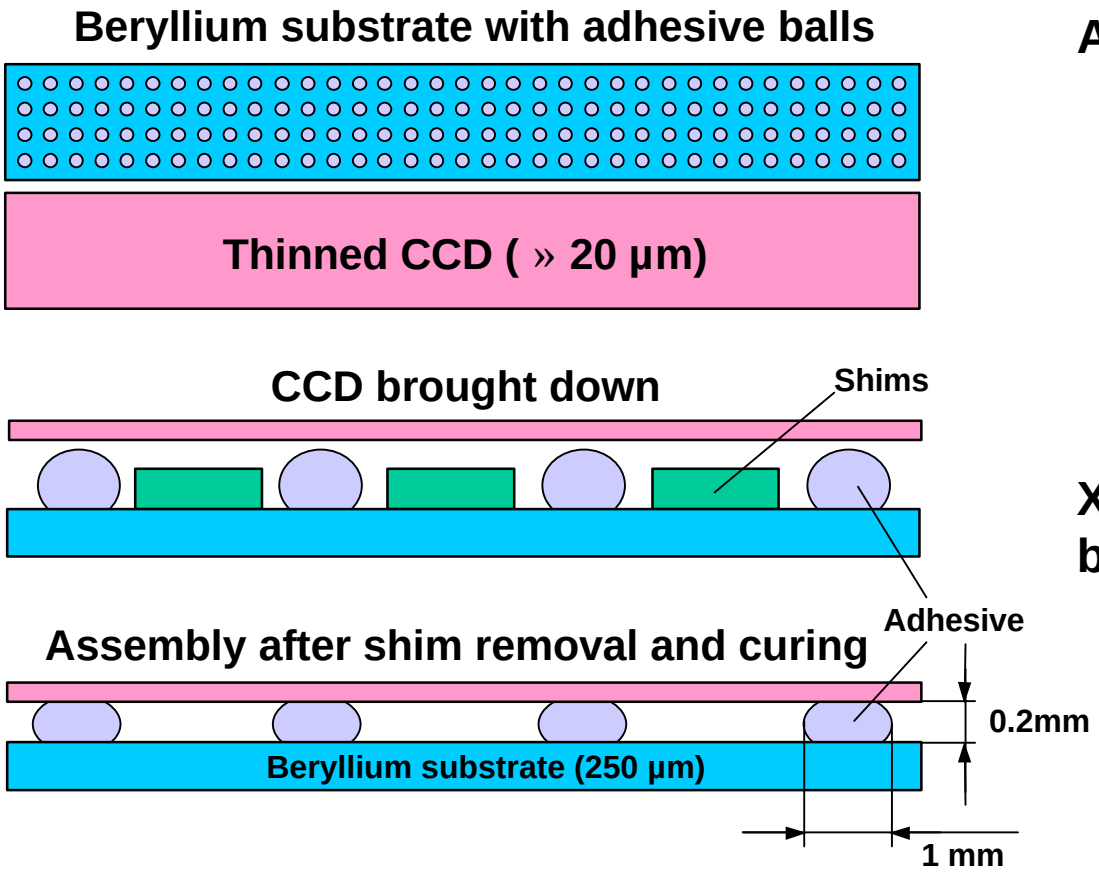
- **Very low mass (< 0.4% X_0 – SLD VXD3)**
- **Shape repeatability to few microns when temperature cycled down to » –100 °C;**
- **Compatible with bump bonding;**
- **Overall assembly sufficiently robust for safe handling with appropriate jigs;**

Three options:

- **Unsupported CCDs – thinned to » 50 μm and held under tension**
- **Semi-supported CCDs – thinned to » 20 μm and attached to thin (and not rigid) support, held under tension;**
- **Fully-supported CCDs – thinned to » 20 μm and bonded to 3D rigid substrate (e.g. Be)**

Semi-supported option





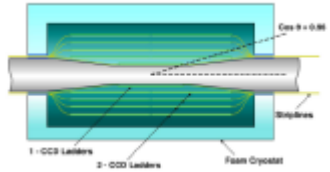
FEA simulations using ALGOR and ANSYS:

- **Distortions only few µm, optimise adhesive pitch and size;**
- **Silicone adhesive: NuSil, excellent at low temperature**
- **Layer thickness » 0.12% X_0**

XY stage for 2-dimensional profiling being assembled:

- **Laser displacement meter**
- **Resolution 1 µm**
- **Models made from steel + unprocessed Si will be measured**

Summary



- **Detector R&D work at the LCFI collaboration:**
  - ♦ **Development of very fast column parallel CCD and its readout chip;**
  - ♦ **Study the performance of commercial CCDs with MIP-like signals at high speeds and radiation damage effects in them;**
  - ♦ **Precision mechanical support of thinned CCDs.**
- **Most aspects of the R&D are applicable to all proposed LC machines;**
- **Work on high speed CPCCD is mainly for TESLA, however the CCDs for NLC/JLC may benefit as well;**
- **Significant R&D is required, challenging combination of chip size and speed;**
- **Have to work hard, R&D is extensive and complex;**

More information is available from the LCFI's web page: http://hep.ph.liv.ac.uk/~green/lcfi/home.html